SEMICONDUCTOR DEVICE WITH MOS TRANSISTORS WITH AN ETCH-STOP LAYER HAVING AN IMPROVED RESIDUAL STRESS LEVEL AND METHOD FOR FABRICATING SUCH A SEMICONDUCTOR DEVICE

Abstract of the Disclosure

A semiconductor device includes a substrate, MOS transistors in the substrate, and a dielectric layer on the MOS transistors. Contact holes are formed through the dielectric layer to provide electrical connection to the MOS transistors. An etch-stop layer is between the MOS transistors and the dielectric layer. The etch-stop layer includes a first layer of material having a first residual stress level and covers some of the MOS transistors, and a second layer of material having a second residual stress level and covers all of the MOS transistors. The respective thickness of the first and second layers of material, and the first and second residual stress levels associated therewith are selected to obtain variations in operating parameters of the MOS transistors.